Layer 0 hybrid

A.Nomerotski Production Readiness Review

Outline

- History
- Design
- Prototypes
- Results
- Documentation
- Summary

Will show here some older slides with relevant information – sometimes language there may be out of date (future tense for things that already happened)

History of L0 hybrids

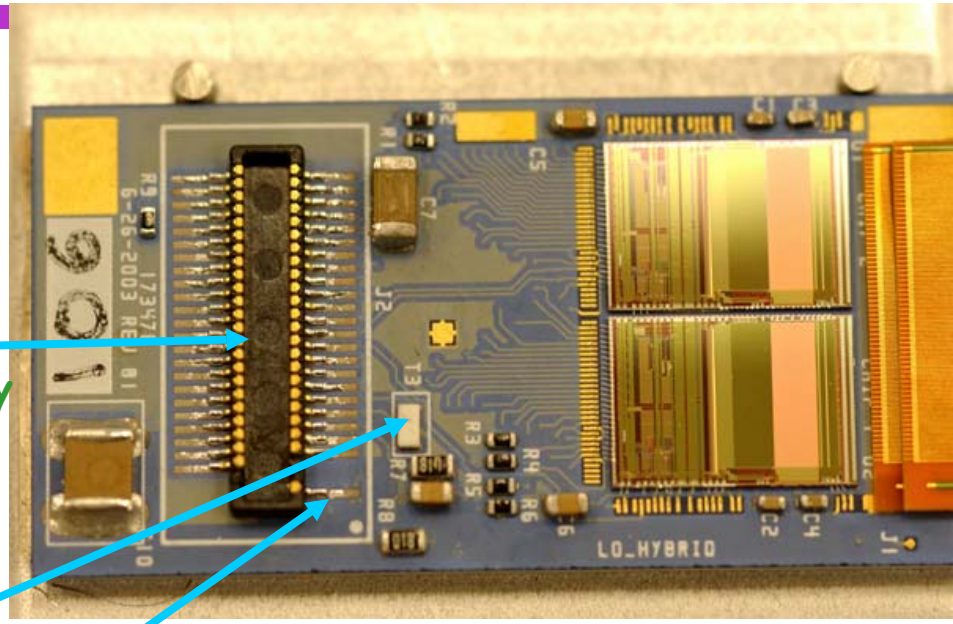
- Rev.1
  - Started design summer 2002
  - Ordered 50 hybrids December 2002
  - Received 22 hybrids May 2003
- Rev.2 : some major changes wrt Rev.1
  - Changes implemented March 2003
  - More changes implemented June 2003
  - Ordered July 2003
  - Received October 2003
- Rev.3 : only small changes wrt Rev.2
  - This is what we are reviewing now

Hybrid design

- Based on Beryllia ceramic
  - Minimize material, BeO thickness 0.38 mm
  - Good heat conductor
  - Established technique
- Multilayer structure on the substrate
  - six Au layers
    - GND & power planes, 4 um thick
    - Traces, 8 um thick, 100 um wide
  - five 40 um dielectric layers, total thickness 0.9 mm
  - Three technologies for vias in dielectric
    - Etching (Fodel dielectric), min via size 4 mils
    - Pattern diffusion, min via size 5 mils
    - Screen printing, min via size 8 mils
  - Screen printing is our baseline
    - Cost effective
    - More vendors capable to screen print on BeO
      - CPT, Oceanside CA - used by CDF
      - AMITRON, North Andover MA
      - Halcyon, LA CA
      - Scramton, LA CA

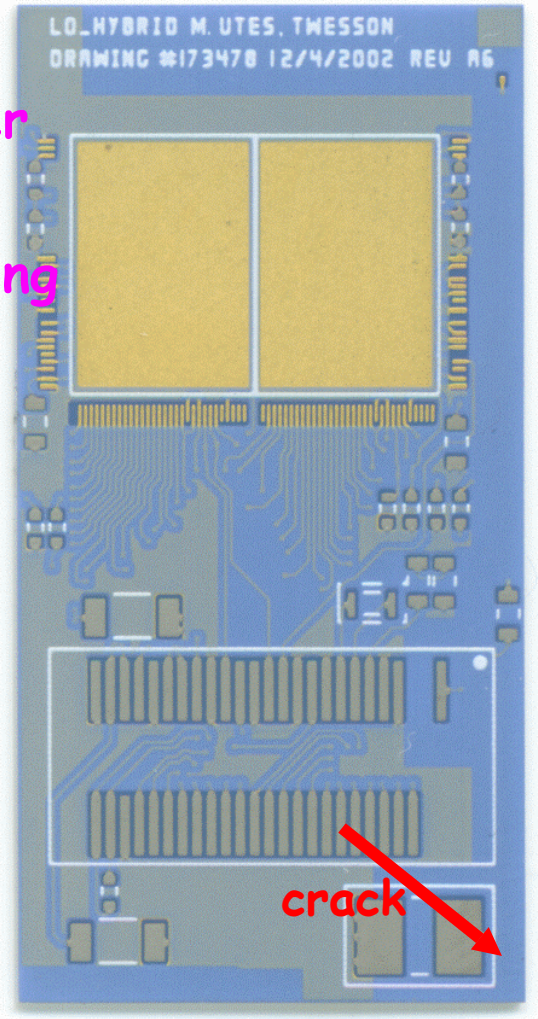
Hybrid design

- Single type of hybrid
  - 2 SVX4.2B chips
  - ~10 mil spacing between vias
  - 50 pin connector
    - Allows for easy testing during all phases of production and assembly
  - Fingerless design
  - bypass capacitors, termination resistors
  - temperature sensor
  - HV routed to side pin with 4 neighbors removed, tested to 1600 V
  - Reserved space ("nuts") for assembling purposes



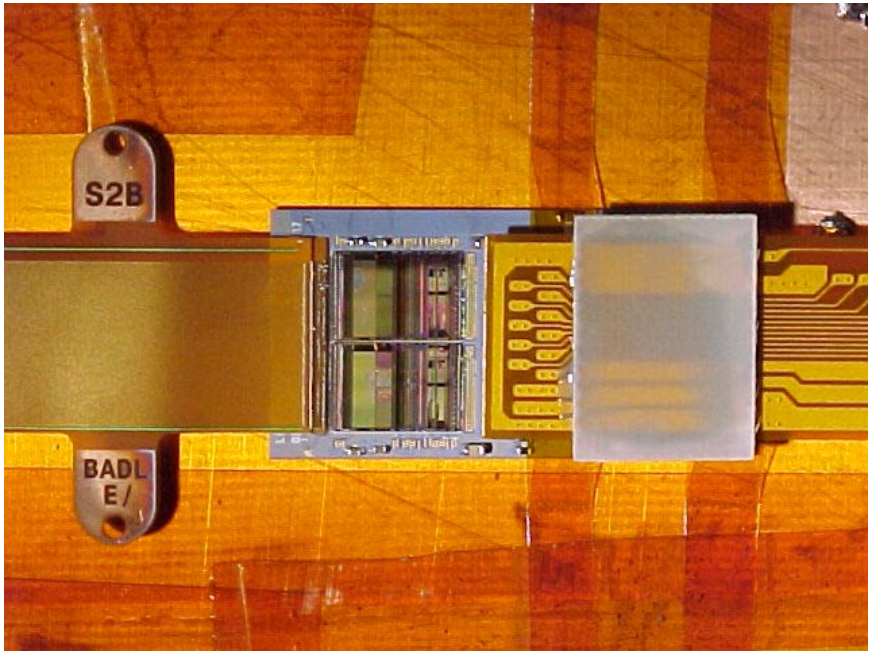
Rev.1 L0 hybrids

- Layout done by T.Wesson
- Manufactured by Amitron
  - Went through internal prototyping of top layer
- 50 hybrids did not pass Amitron QA
  - A few mm long crack in the corner during dicing
  - Electrical tests ok
  - Amitron started new lot
- Received 22 hybrids for free, inspected two
  - Crack ~10 micron wide
  - Does not cross artwork
  - Dimensions are ok
    - Flatness 20-40 um (spec 100 um)
    - Thickness 750 um (spec 800 um)
- Can be used for L0 prototypes
  - will stuff several hybrids

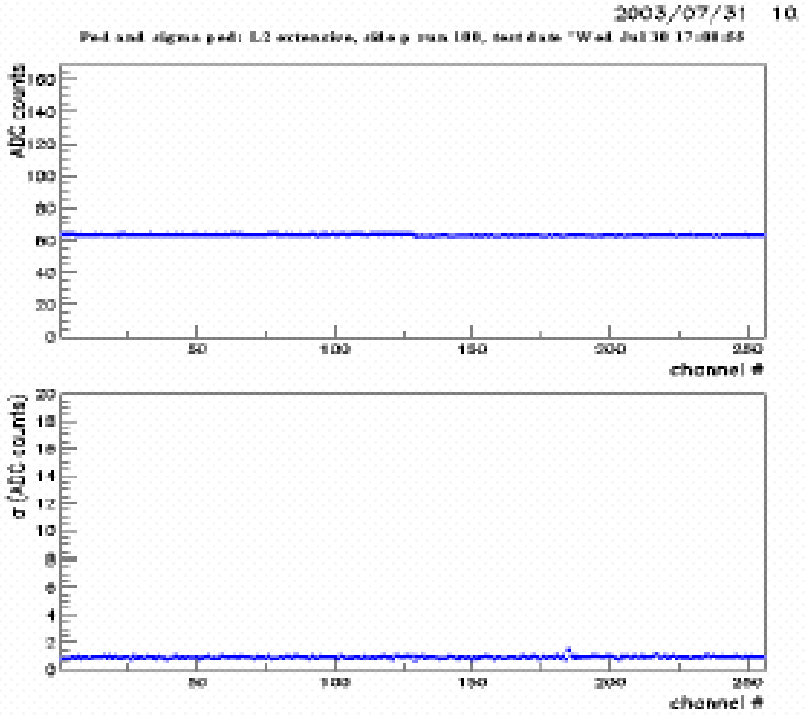


Rev.1 L0 hybrids

- Stuffed 10 hybrids
- Used for L0 prototypes



Pedestals and Total noise



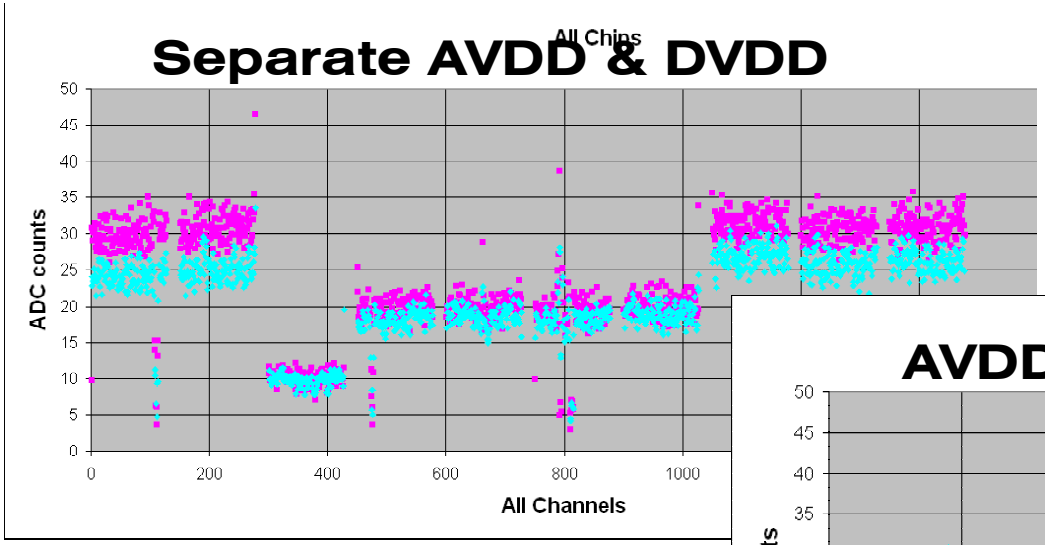
Hybrids : revision 2

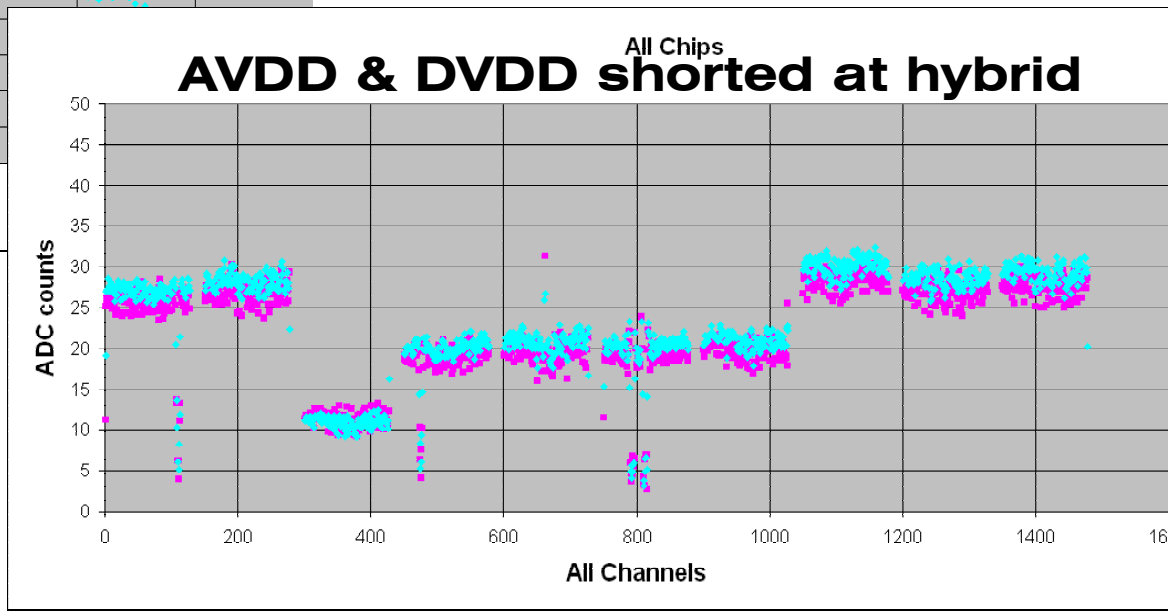
Rev.2 implemented major changes - reviewed below

- We are ready for next revision of the hybrids
  - specs for the SVX4.2A and SVX4.2B are frozen
  - SVX4 output interface is not changing
  - testing of the rev.1 hybrids mostly complete
- Mechanical issues
  - Bonding tested OK
  - mechanical dimensions OK
  - agreed on the nut locations - some surface components will move

Hybrids : revision 2

- **Electrical issues**
  - Combined AVDD and DVDD power
  - Tested noise at bare hybrid and L2A 20-20 module - OK
    - total noise is a bit better with combined power



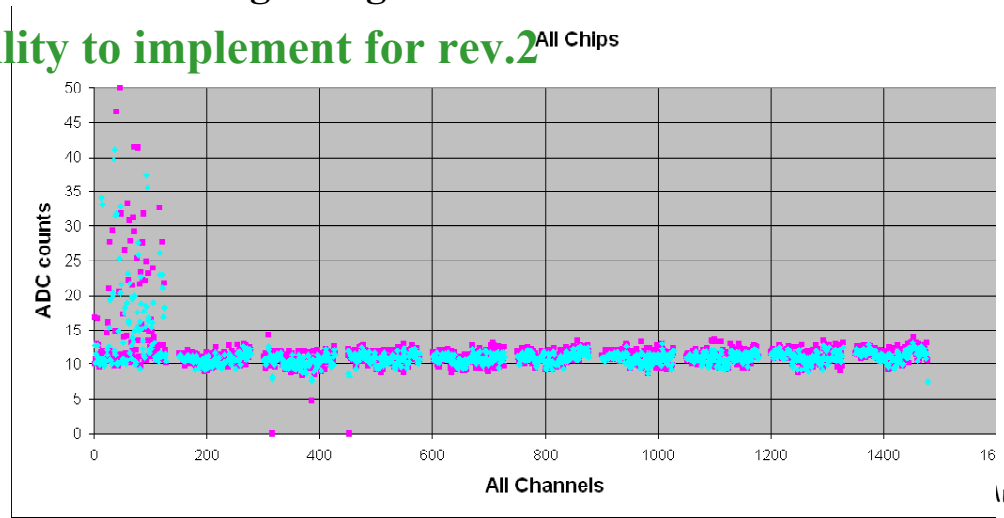


Hybrids : revision 2

- **Electrical issues : combined AVDD & DVDD**
  - **Have common GND and combined AVDD & DVDD return anyway**
  - **SVX4 designers (Tom Zimmerman) recommend common power**
  - **Will allow better referencing of signal traces on the hybrid**
  - **Will allow use mesh for the power layer (=>less material)**
  - **Will simplify hybrid, adapter card and power supply designs**

Hybrids : revision 2

- **Power bypassing**
  - Checked voltage variations as function of bypass
  - voltage variation can be decreased increasing the bypass
    - no effect on the noise for hybrids
    - found bigger capacitors, same size (10 uF vs. 2.2 uF)
    - need to check noise performance of L2A 20-20 as function of bypass
  - Designers recommend different way of DVDD bypassing
    - checked on 10-chip hybrid - no effect on noise (chips 1 and 6 modified)
      - Chip 1 was bad from the beginning
    - will study possibility to implement for rev.2



Hybrids : revision 2

- **Preamp BIAS bypassing**
  - Power supply rejection can be optimized by two capacitors, one to AVDD, one to GND
  - Large capacitive load requires C to AVDD (like in present hybrid)
  - SVX4.2B will have on-chip BIAS bypass to AVDD
  - if the above works it can be left unloaded
    - in any event TZ claims this bypass is not relevant for D0 operation
- **Terminations**
  - Studied with full chain, presented at the December workshop
    - Differential signals : source termination at AC
    - Single ended signals : can use source termination as well - removes 3 resistors from the hybrid
- **VCAL : remove serial 100 Ohm**
- **Remove as much material as practical from the top ground layer**

Hybrid Flatness

- Topic mostly important for bigger L2-5 hybrids – present here for completeness
  - Flatness spec for L0 hybrid 150 um

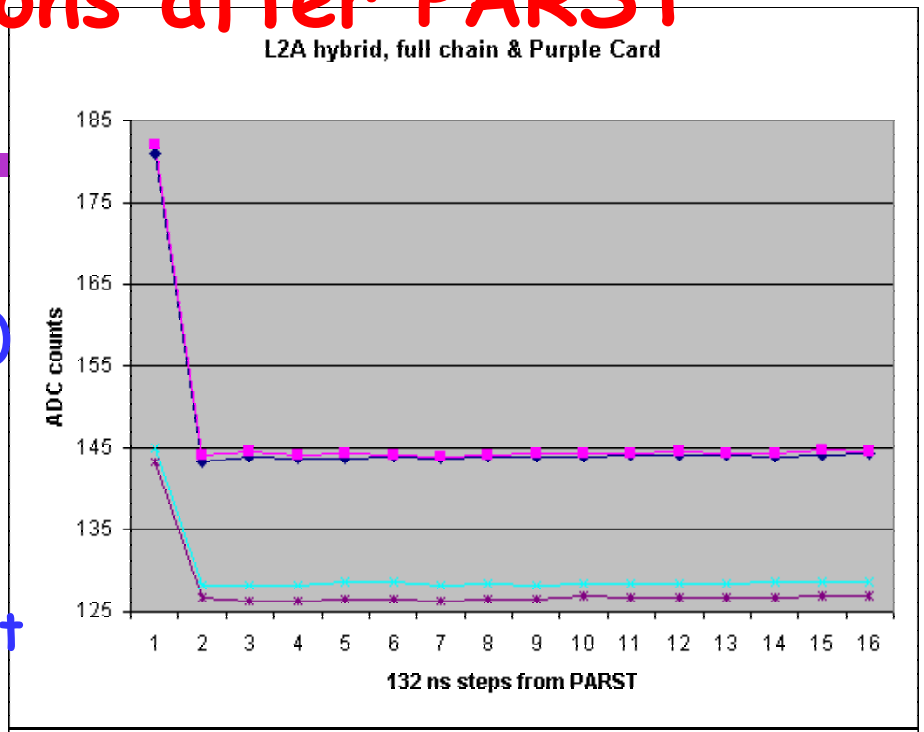
- Original specification for flatness was 50 um
  - Not perfect CTE matching of BeO and dielectric (including different temperature dependence) causes bending during firing cycles – known effect
  - To compensate some dielectric is printed on the other side of BeO substrate
    - Limitations : Total thickness spec (0.95 mm) and processing issues
  - Another approach tried by CPT is lapping
- Three first batches from CPT were close to the spec while two last batches failed
  - Reason not understood, apparently 50 um spec is too tight
- After discussions with mechanical group decided to increase the flatness spec to 150 um
  - Gluing to silicon is less trivial but possible – tests successful
  - Silicon temperature ok even with partial glue coverage (up by 2 degC max)

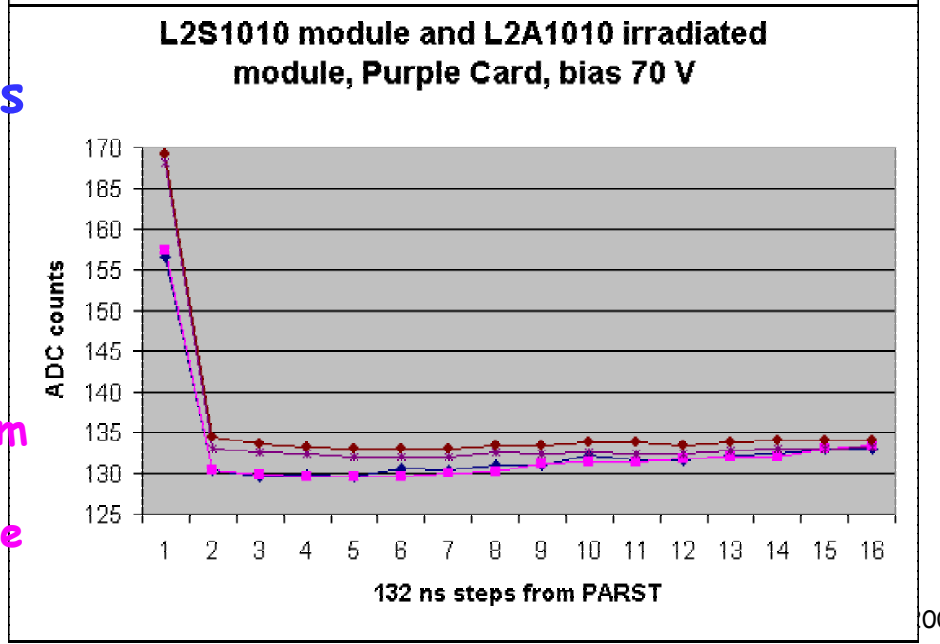
More changes to rev.2 layout

- All motivated by worries about grounding
  - Effects seen in Run2A detector
  - Found attractive scheme for handling of analog and digital powers (Howard Johnson scheme)
  - Developments in understanding of L0 CF support structure

Oscillations after PARST

- In SMT see ~ 2 ADC counts oscillations as function of distance to PreamReset (PARST)
  - May be coming from GND oscillation – reason of concern and recent discussions
- Bare SVX4 measurements does not see this (see Kazu's slides at 2/24/2003 meeting)
- Done measurements addressing this for 10-chip hybrids/modules
  1. With Purple Card (top curves)
  2. With full chain (bottom curves)
  3. For non-irradiated and irradiated module
  - No oscillation seen
  - Slope 1-2 ADC counts expected from the pipeline slope in rev.1 SVX4
  - Irradiated module had 3 counts slope – investigating



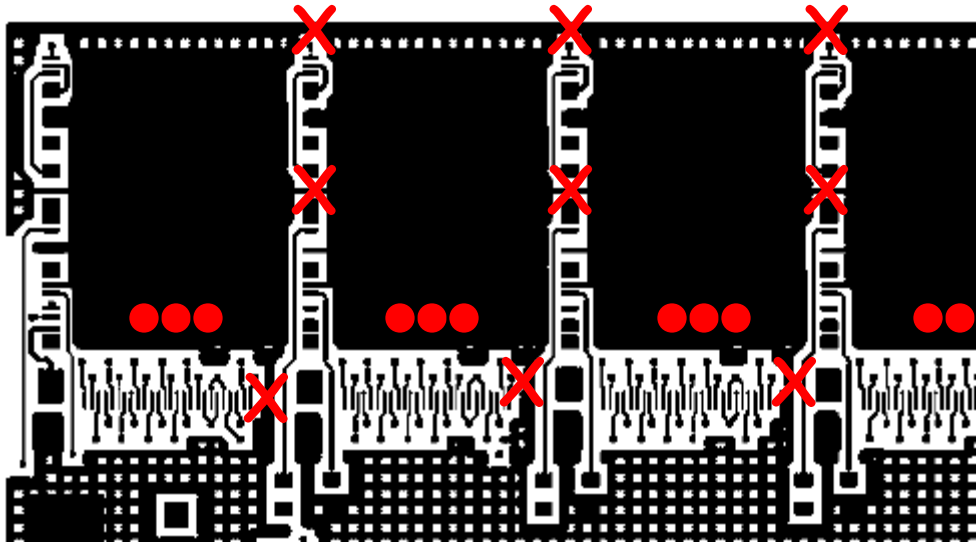


Changes in Hybrid Ground

- Reviewed ground configuration for rev.2 hybrids (J.Anderson, M.Johnson, M.Utes, J.Green, AN)
  - Before had a common ground allowing for digital currents under SVX4 chips
  - Single point analog and digital ground connection near SVX4 is best theoretically. For multi-ADC design the implementation is less straightforward but in any case maximum isolation of analog ground is recommended.
  - Decided to modify hybrid top metal layer to isolate analog ground of each chip (following H.Johnson's recipe on multiple ADC grounding) and also to provide low inductance pass for digital ground by multiple bond connections.

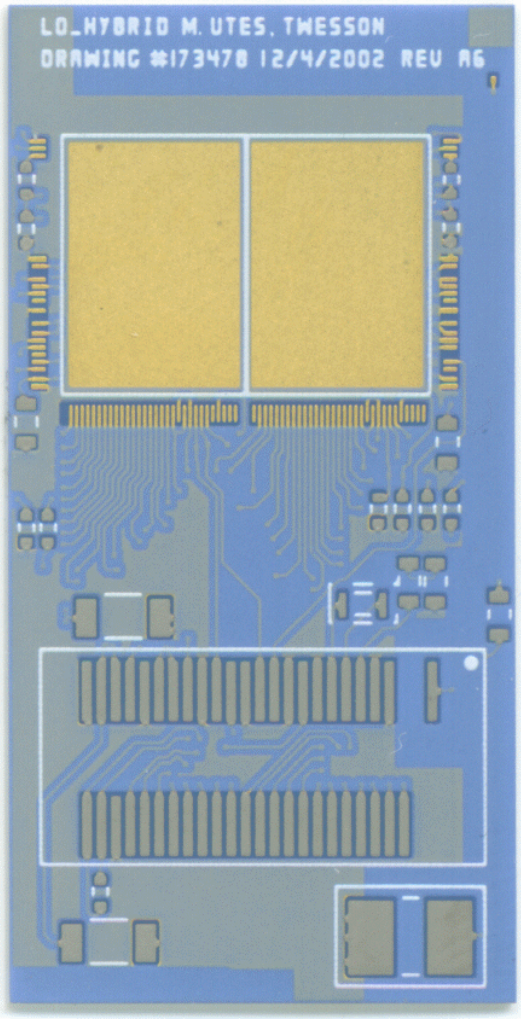
Changes :

1. Break ground bridges between chips and from chips to mesh ground (red crosses)
2. Have 3 vias (red dots) from the chip ground to ground plane (last metal layer)
3. Bond digital grounds from both sides of SVX4

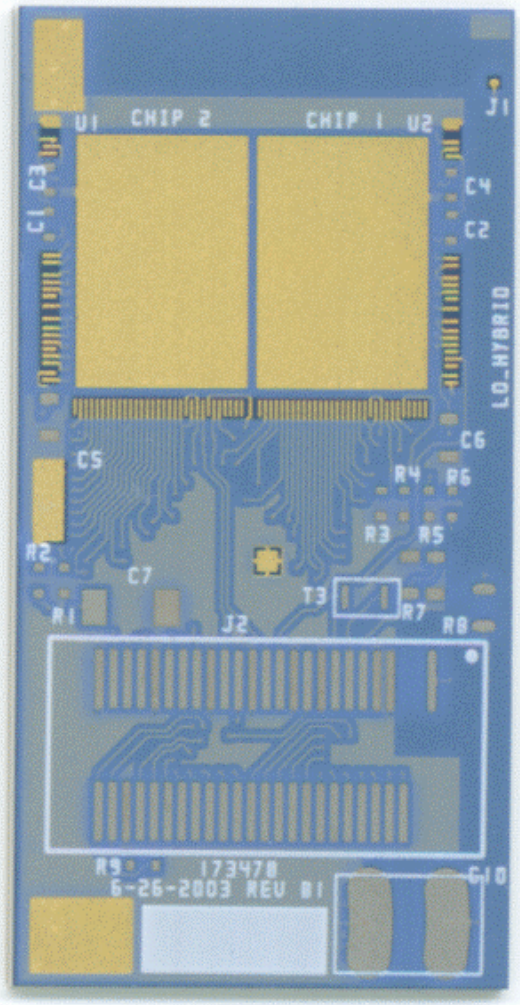


L0 hybrid

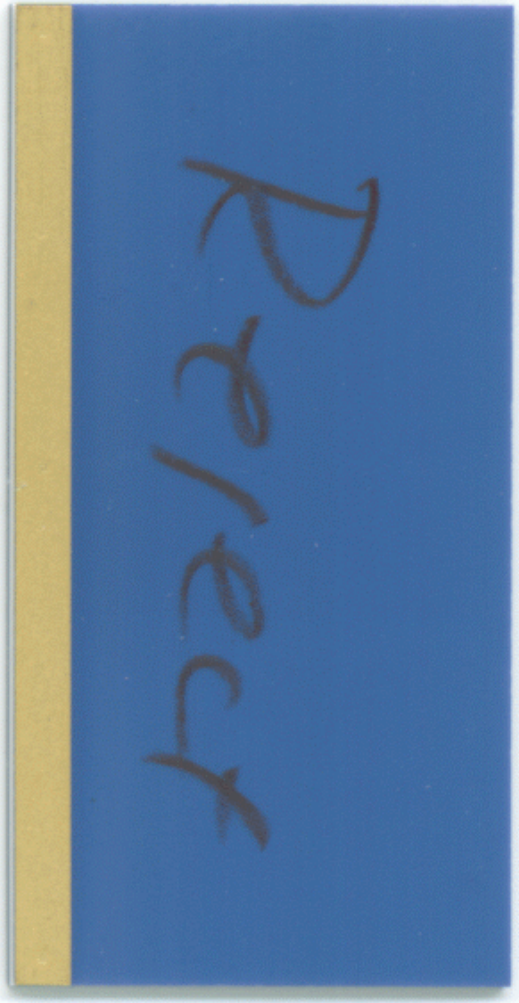
- Rev 1



Rev 2



Rev 2 backside



Rev.2 L0 Hybrids

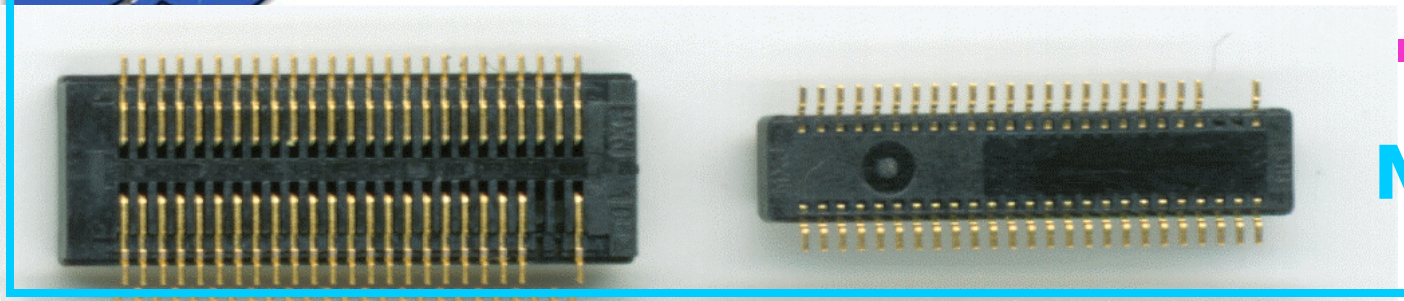
- Rev 2 Layout done by T.Wesson at Fermilab
  - Has vias in Be substrate to connect to GNG strip on the back of hybrid
- Amitron wanted to redo the Rev.1 order
- Order for Rev.1 L0 hybrids stopped at Amitron and substituted by the new design (i.e. rev.2) end of July 2003
- Hybrids delivered end of October
  - 25 good + 5 rejects
  - Delivery slipped by ~ one month
  - 3 month turnaround was one of the fastest anyway

Rev.3 hybrid

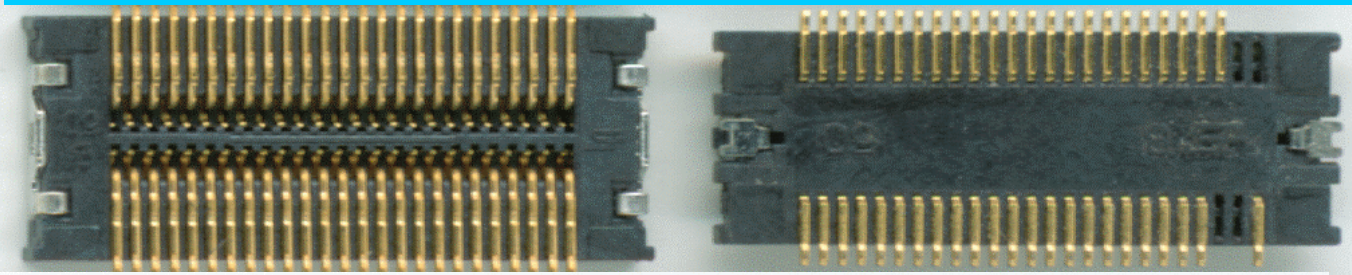
Minor changes – reviewed below

- 1.5 mm MOLEX connector
  - Same pitch 0.5 mm
  - Can be soldered to rev 2 L0 hybrid – needs tests
  - Smaller dimensions wrt to 2.5 mm AVX
  - Pins easily removable
  - Plastic looks the same (rad/HV issues)
  - Plugging / unplugging ok

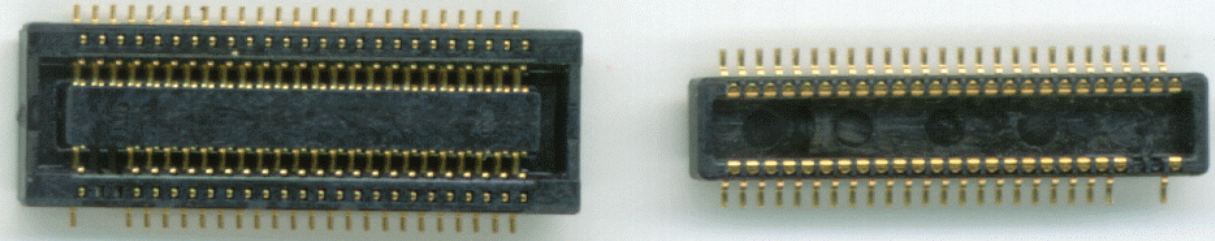
Connectors



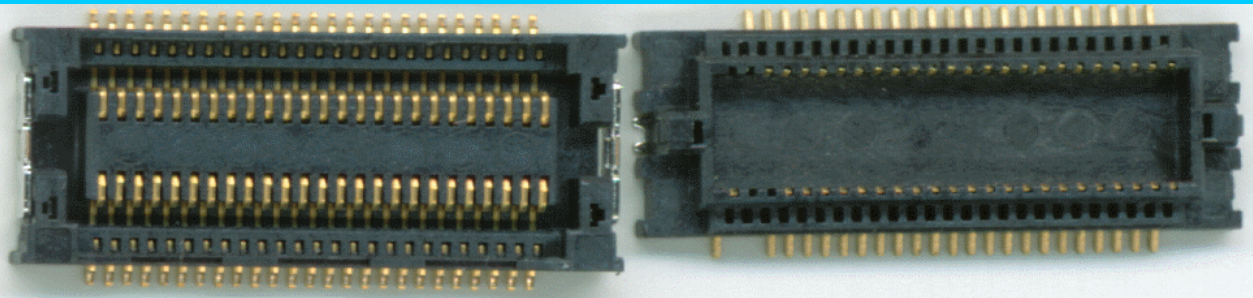
MOLEX



AVX



MOLEX



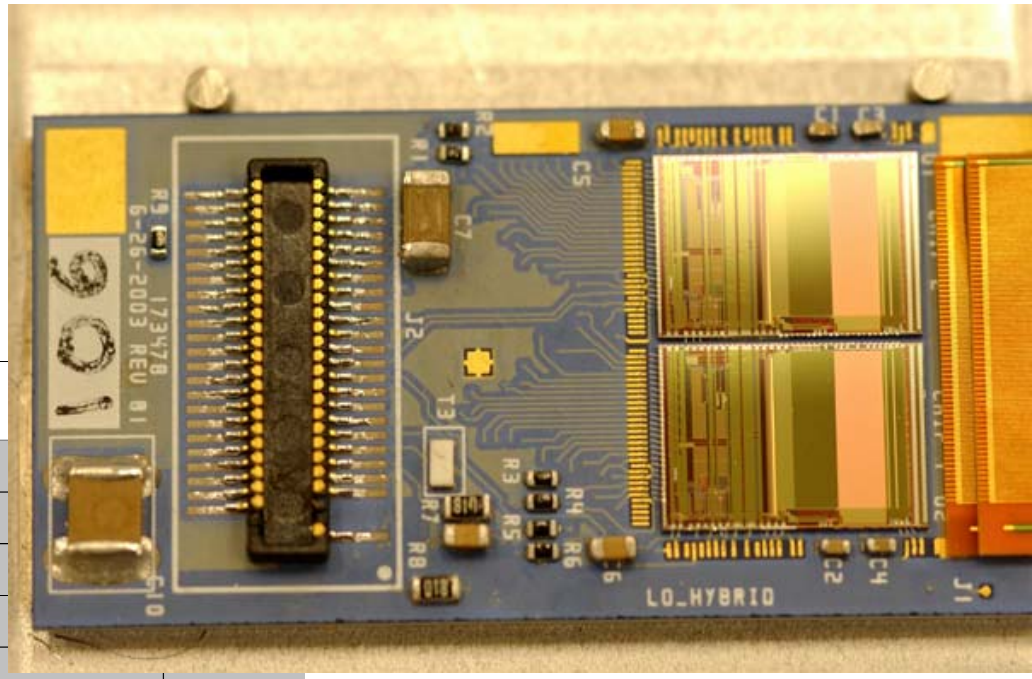
AVX

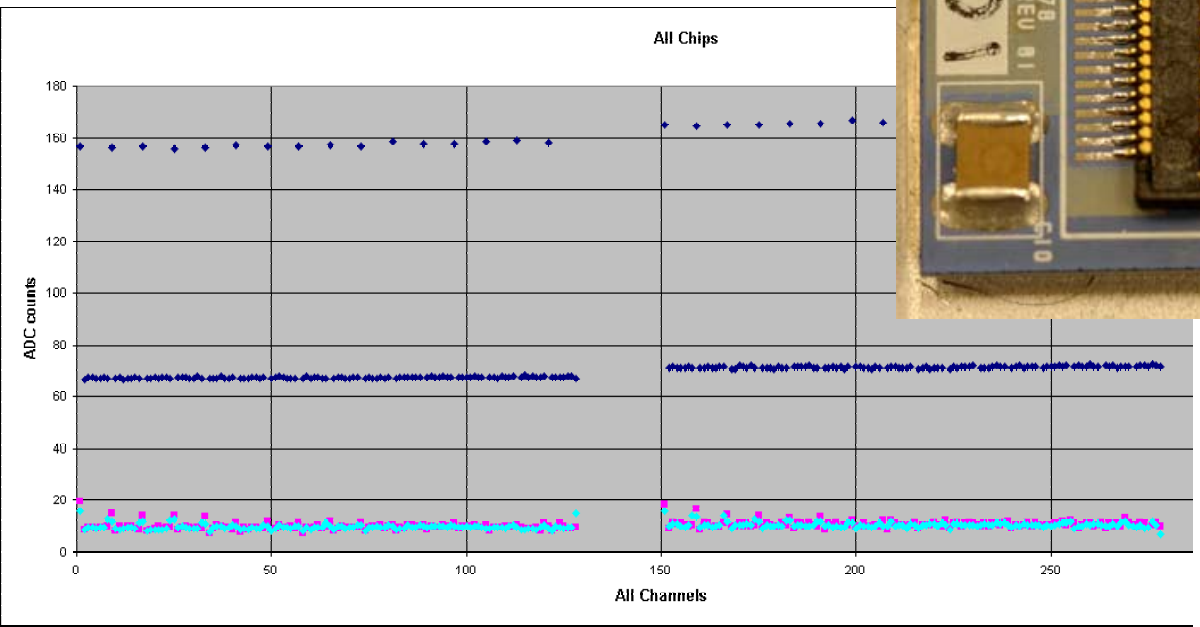
Rev.3 L0 hybrid

- Went through many iterations for the revised layout with Tom Wesson
  - The only issue with rev.2 hybrid was size of solder pads which needs to be increased
    - Done
  - Central fiducial may need to be moved
    - Done
  - Doing the above had to move many traces and vias – final version needs careful checks
- Reviewed each version of layout internally (MU, JG, AN)
- Layout is out for a wider internal review
- Revised specs are being prepared
  - May want to leave 2 mm strips on the back side without dielectric prints to improve the hybrid cooling
    - The dielectric prints are needed to compensate for bending
    - Need discussion with Amitron
- Ready for PRR

Rev.2 L0 hybrids

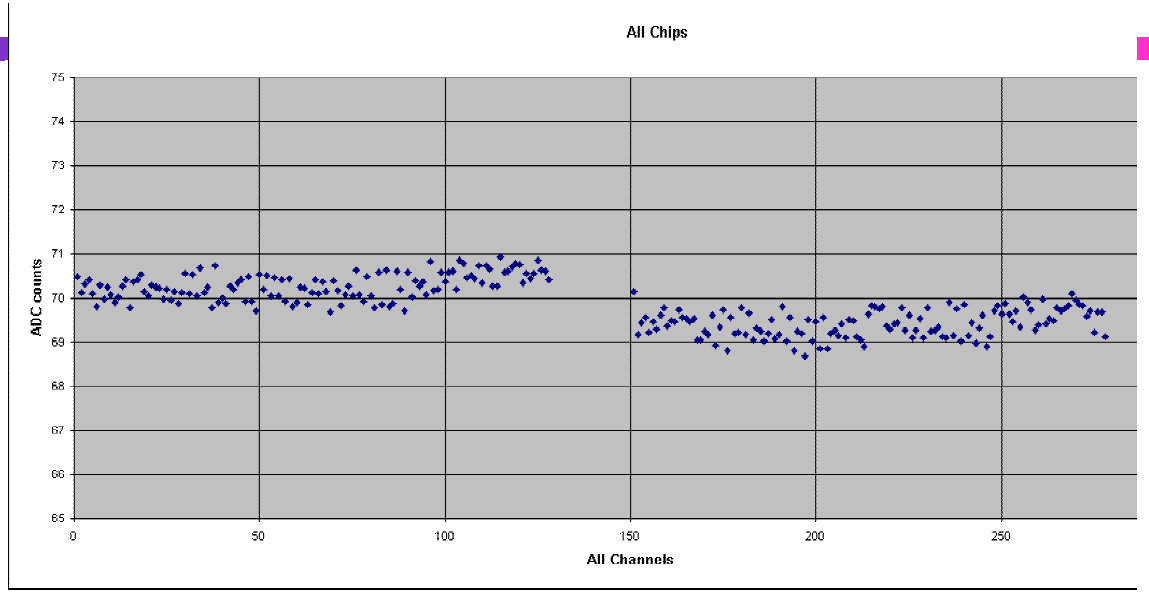
- Assembled and tested 12 new L0 hybrids
  - Used latest revision of SVX – SVX4.2B
  - Used 1.5 mm profile MOLEX connector planned for new Layer0
- Results are very good
  - Noise 1 ADC count
  - Flat pedestals
  - Plot below shows
    - Calinjects
    - Total & differencial noise



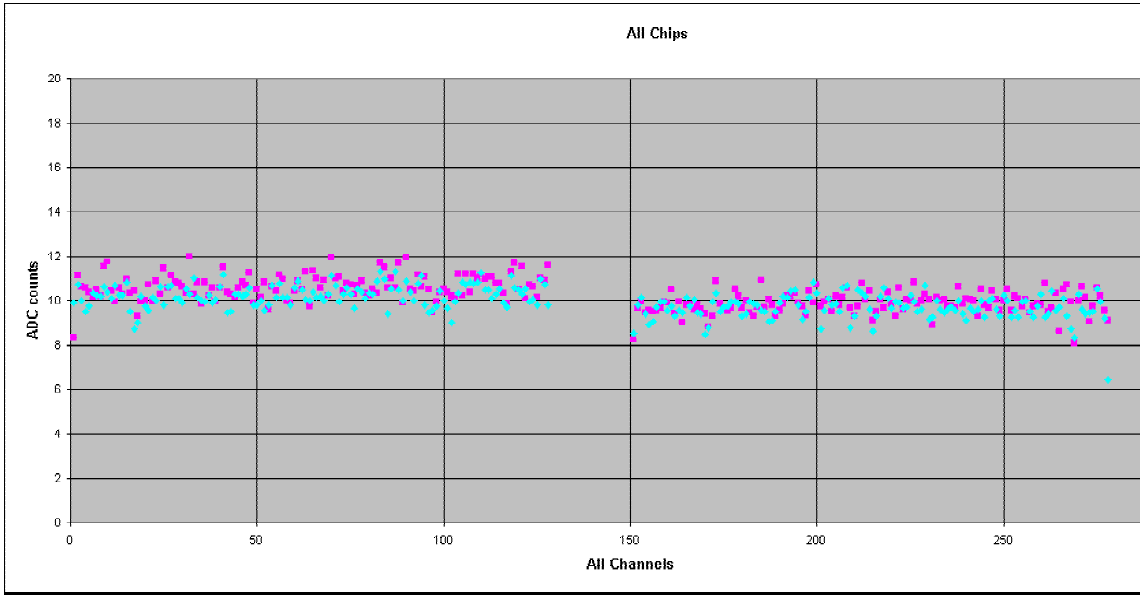


L0 hybrids rev.2

- Pedestal

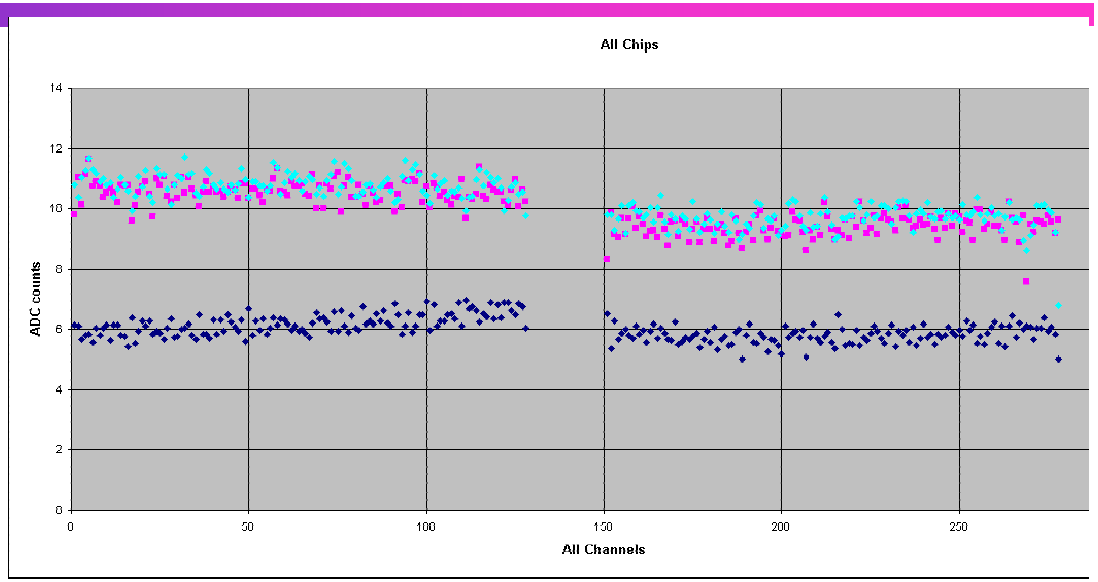


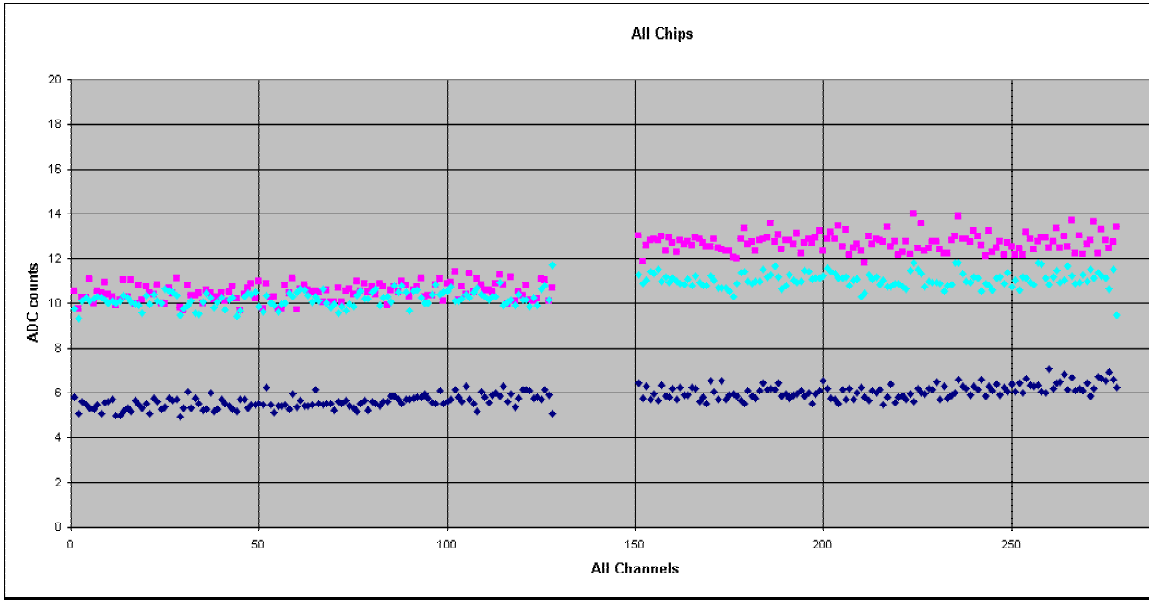
- Noise



L0 hybrids rev.2

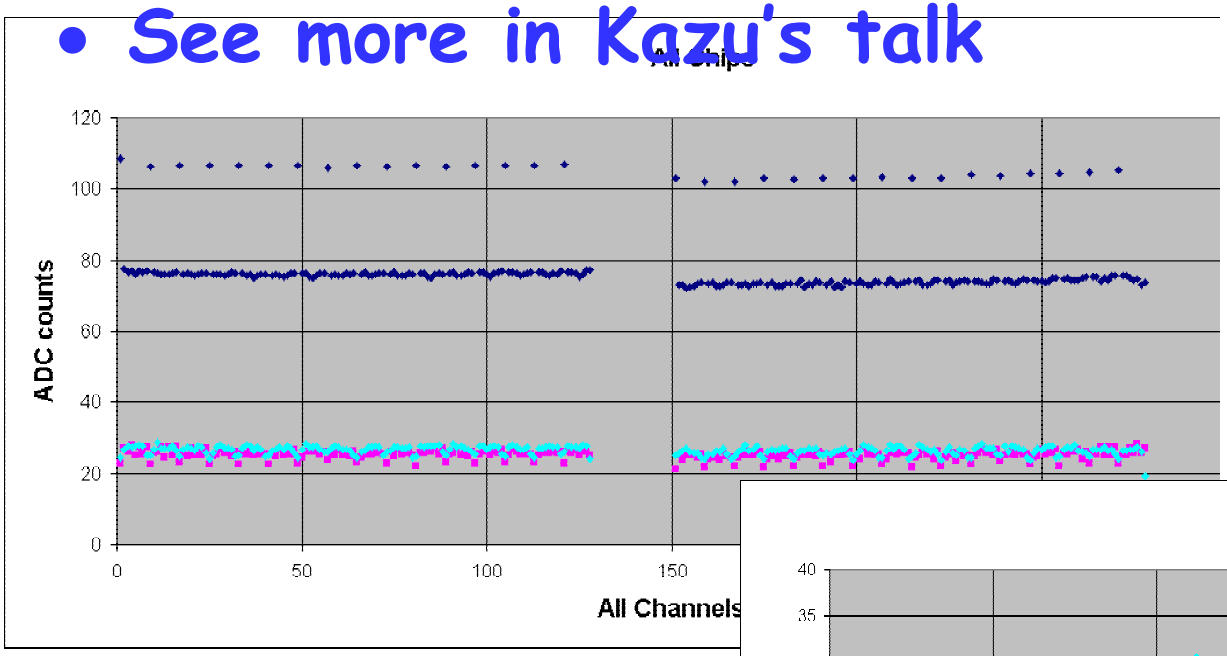
- Dynamic pedestal subtraction ON

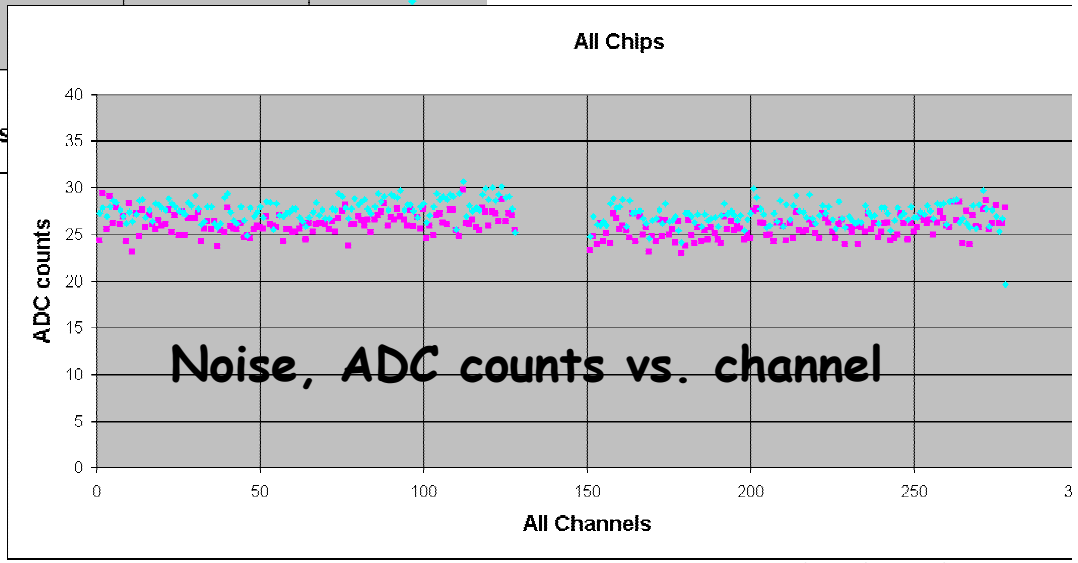




L0 module with rev.2 hybrids

- Good performance – best we ever had
- See more in Kazu's talk





Hybrid testing

- Summary of discussion at KSU in April 2003
  - Hybrids need to be tested as thoroughly as possible before burn-in
    - Chips will be wafer tested but
      - Dicing yield
      - Collective effects
    - Simple things (spreadsheet level)
      - Full parameter space scan
      - Pipeline cell scan
  - Voltage scans
    - VDD scan with Purple Card
    - KU and Fermilab will do R&D to define specs
  - Timing scans
    - KSU and Fermilab will do R&D to define specs
    - DV phase with Purple Card, 2 ns steps
    - Phase of CLK and /CLK
    - Duty cycle of clock
  - Full chain test – partly addresses timing issues above
    - Different length cables : 80-conductor, twisted pair, jumper
    - Main reason why duty cycle is different for different channels
    - Different firmware

Summary of KSU radiation tests

- Hybrid survived 25 MRad
- No significant change in noise performance (result consistent with SVX4 irradiation)
- Slight increase in channel-by-channel scatter of pedestals
  - Pedestal scatter is one of the issues addressed in the next SVX4 version

Documentation

- Production Readiness Review L0 hybrid & Analog Cable

  Hybrid Documentation Package
- latest layout files
  - 4MB .zip file with gerbers and .dwg for all layers
  - 4 MB .zip file with .dxf files for all layers
  - M.Utes Engineering note U040209A "Hybrid Pre-Manufacture Layout Checklist"
- Specifications for vendors
- Bonding diagram .pdf
- Schematics rev.3
- Loading diagram rev.3
- Bill Of Material rev.3
- Assembly procedures for stuffing house
- mechanical drawing, see last page of the specs

Summary

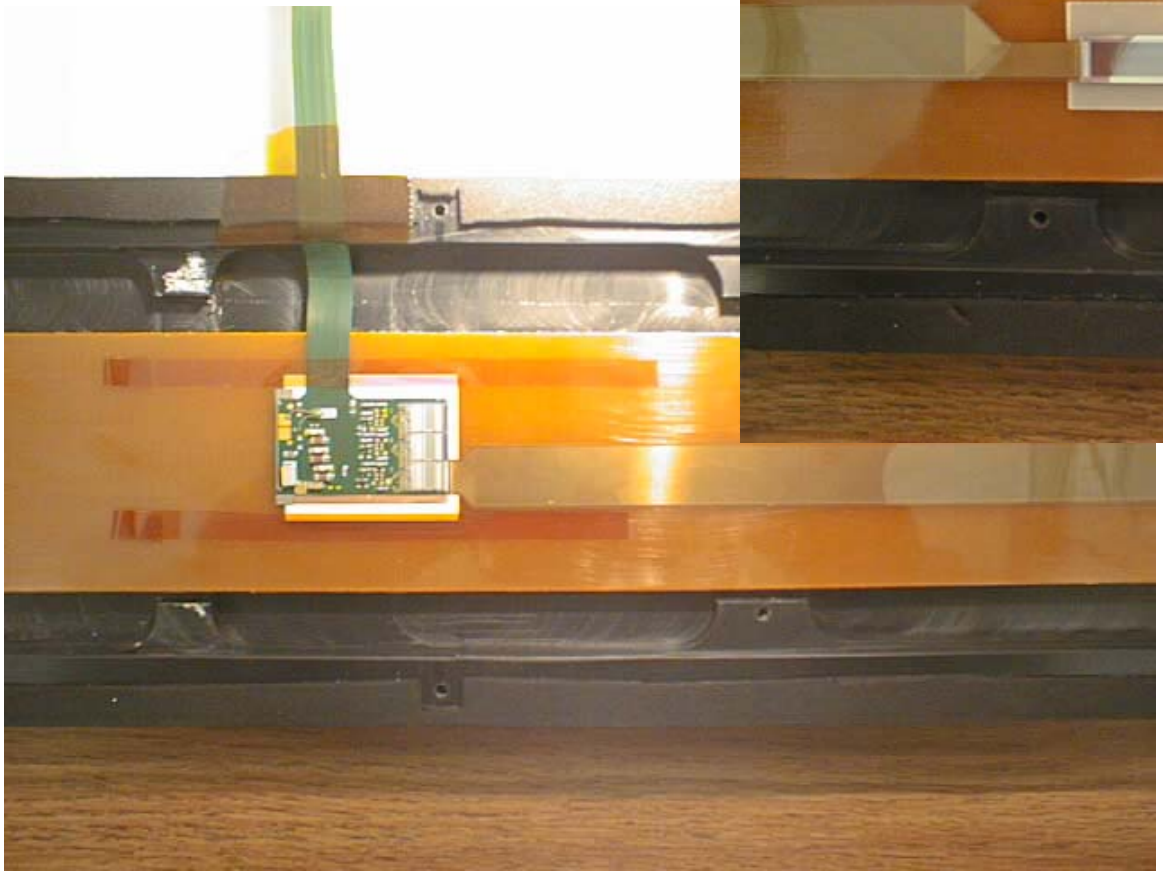
- We are ready for production

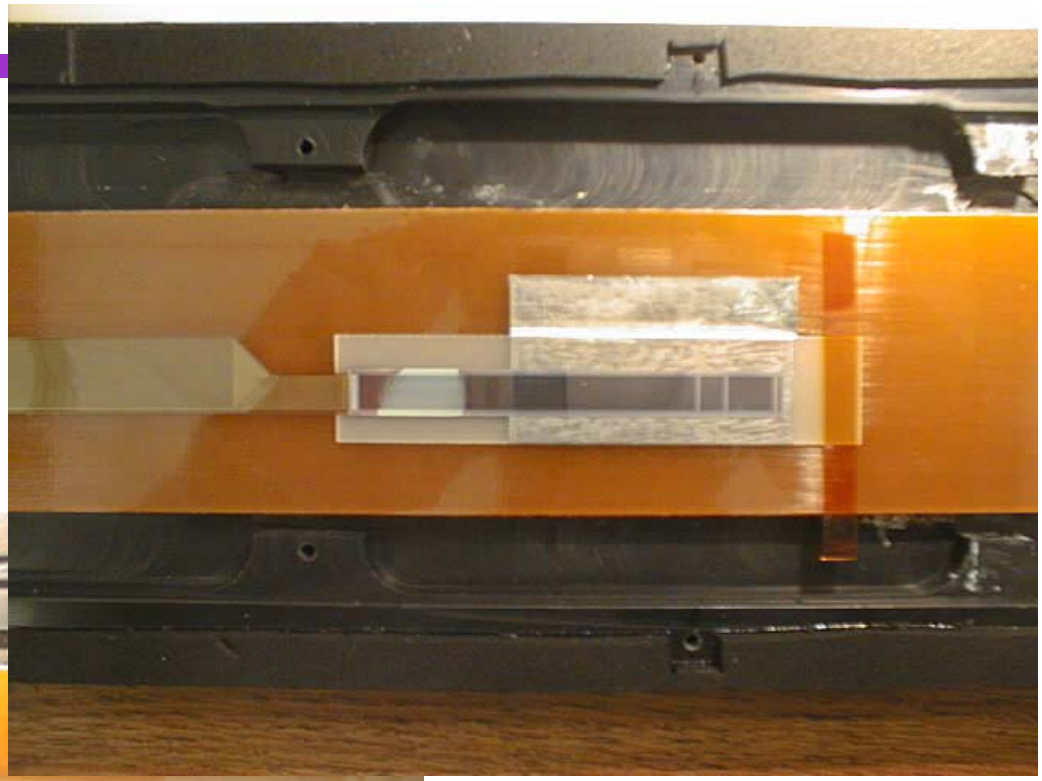
Analog Cable

Outline

- Requirements
- History
- Design
- Prototypes
- Some results
- See also Kazu's talk

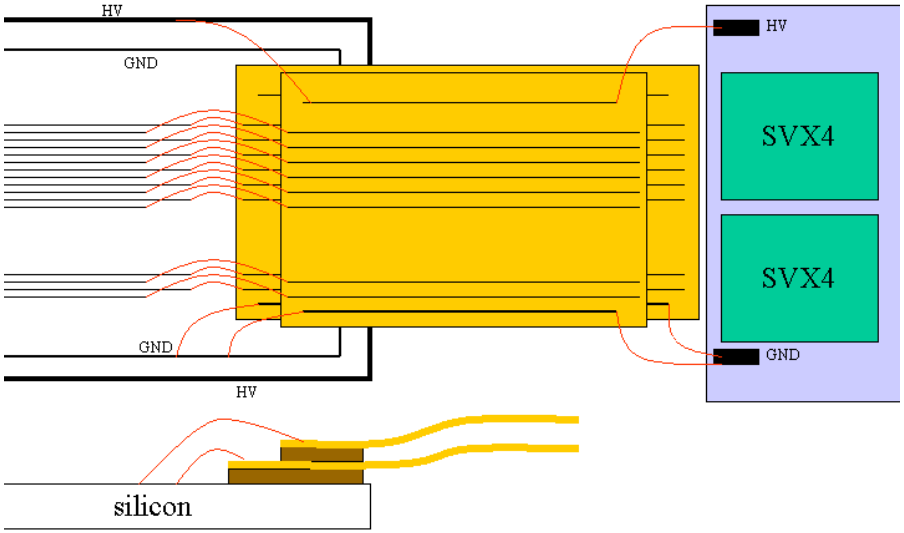
L0 prototype with SVX2 chips and CDF analog cable



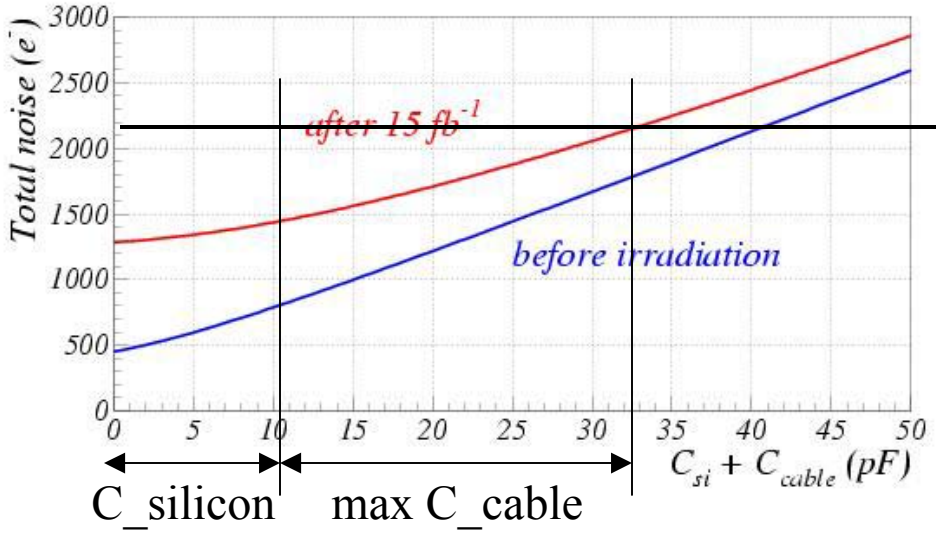


Analog Flex Cables

- Build a prototype with Run2A HDI and CDF style cable – started to think about different design
- Low mass, fine pitch cables for Layer 0
  - Trace width 15-20 um
  - Constant 100 um pitch without fan-out region
  - Two cables shifted by 50 um, effective pitch 50 um matches sensor pitch



L0 noise performance



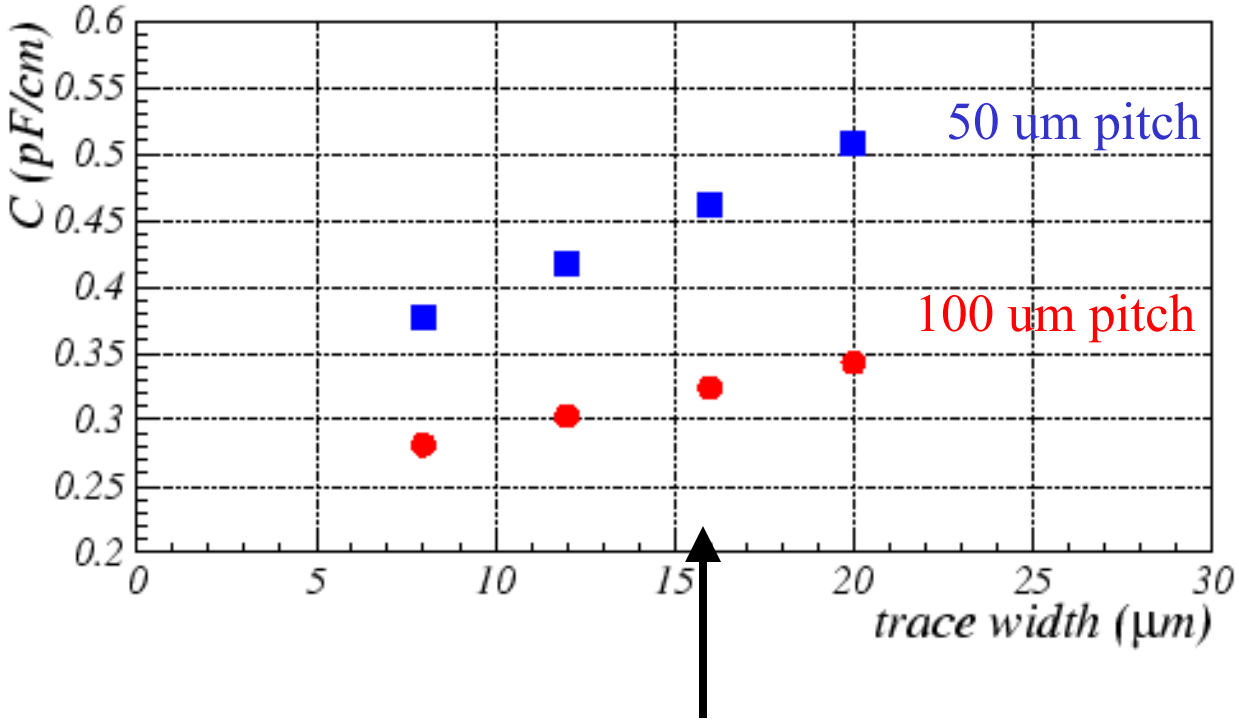
S/N =10

Acceptable cable capacitance is determined by noise performance

S/N = 10 after 15 fb-1 => C_cable < 0.55 pF/cm for 42 cm long cable
typical C_silicon ~ 1.2 pF/cm

Analog Cable Capacitance

- FE calculations (ANSYS) agree with measurements within 10%
- 50 μm thick substrate with $\varepsilon_r = 3.5$
- Settled on 91 um pitch and 16 um trace width



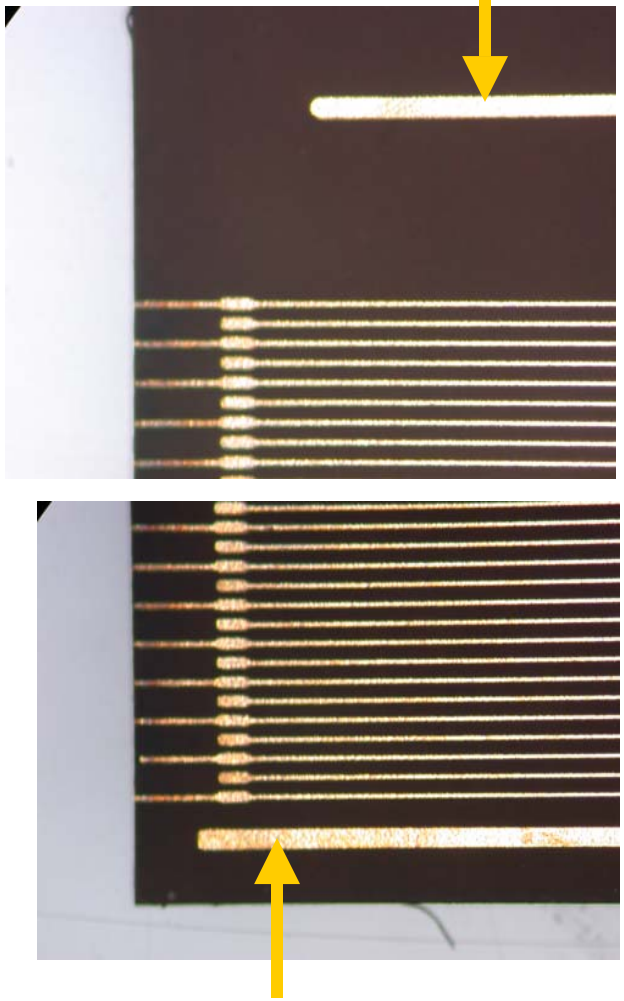
16 um => 0.32 pF/cm

Analog Flex Cables

- Dyconex
  - Designed by Fermilab, Universitaet Zuerich
  - Second prototype run
    - pitch 91 um, trace width 16 um
    - Used regular etching technology
    - March 2002 : 15 mechanical grade cables + 12 good cables
    - July 2002 : 27 good cables
  - Results on 39 prototype cables:
    - Good quality of imaging
    - Allow one open trace out of 129

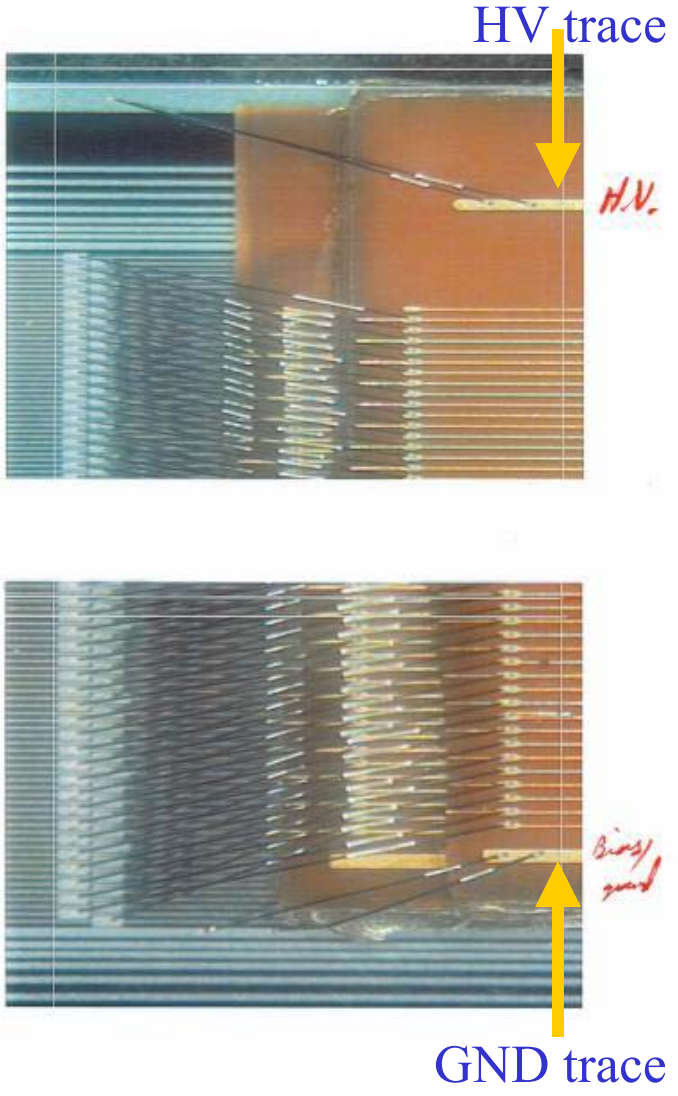
Open traces	0	1	2	>2
cables	22	13	4	0

    - Measured trace width : 10-12 μm
    - Capacitance, resistance measurements under way
      - **Preliminary C=0.35 pF/cm**



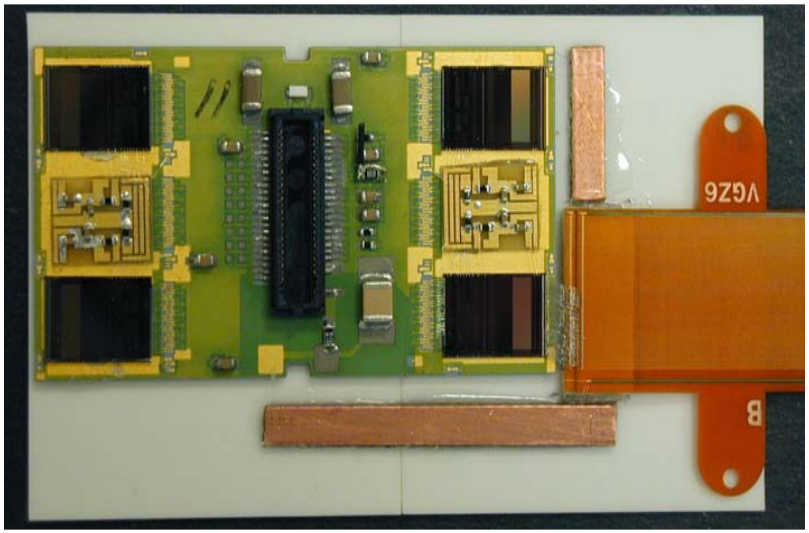
L0 module prototype

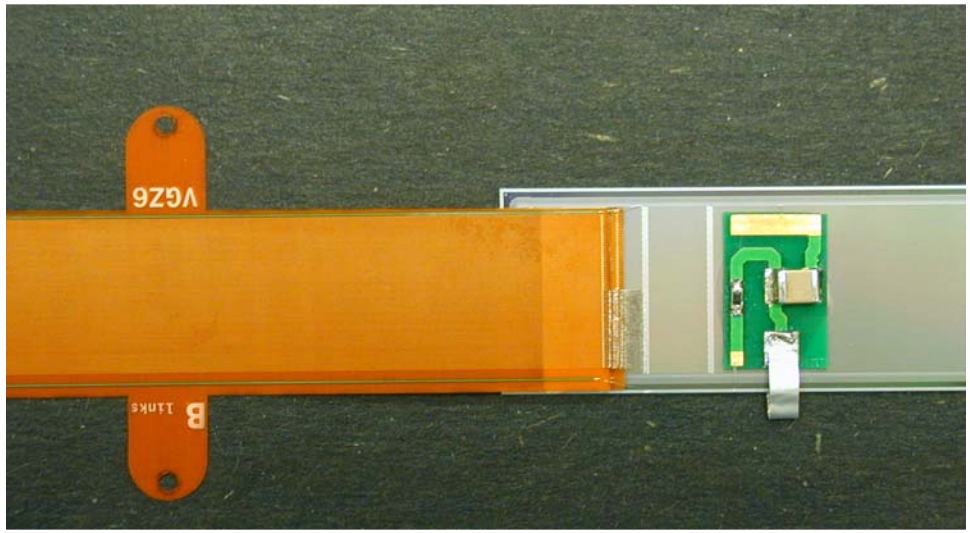
- Built L0 module prototype in May 2002
  - Dyconex cables
  - ELMA L0 sensor
  - Run2A HDI with 3 SVX2 chips
- Proof of principle
  - Simpler approach works
  - Developed handling & assembly procedures
- Measured
  - Noise ~1900 e – agrees with SVX2 performance
  - Shielding geometry studies (next slide)
- Building new prototype with SVX4



L0 module prototype with SVX4

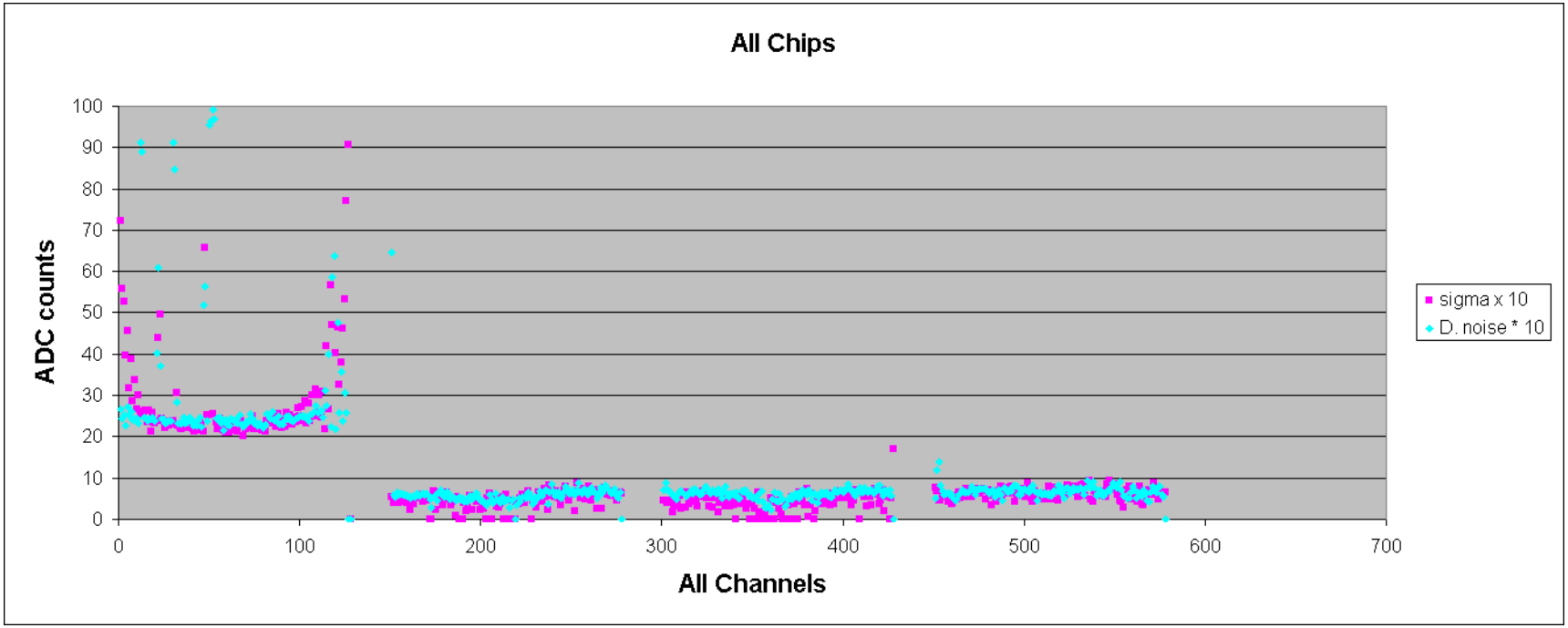
- First L0 prototype with SVX4
  - ELMA L0 sensor, two Dyconex 42.5 cm analog cables
  - L1 prototype hybrid
  - Verification of SVX4 performance
    - With large capacitive load
    - With long antenna on the input





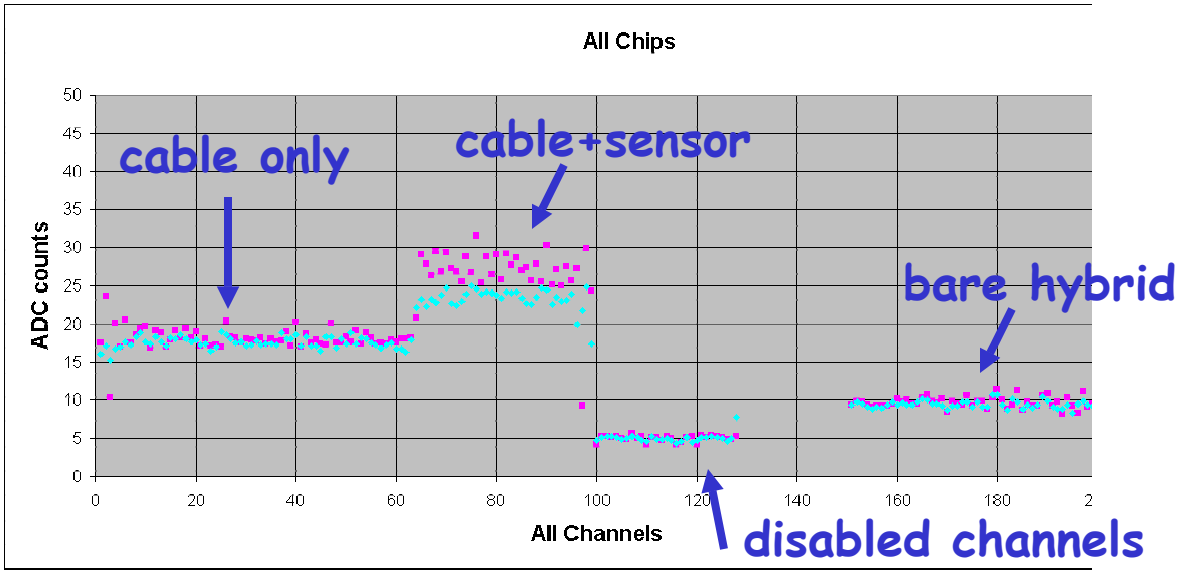
L0 module prototype with SVX4

- Preliminary results
  - Noise ~ 2.3 ADC counts
    - Bare chip 0.7 counts



L0 module

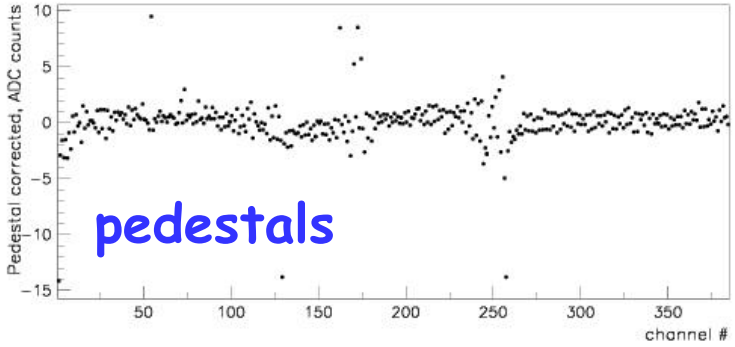
- Noise studies with L0 structure (Kazu H, Daekwang)
  - Noise vs. two cables separation
  - Shielding/Grounding effects
  - Noise vs. distance to shielding
- Low inductance connection gives low common mode noise

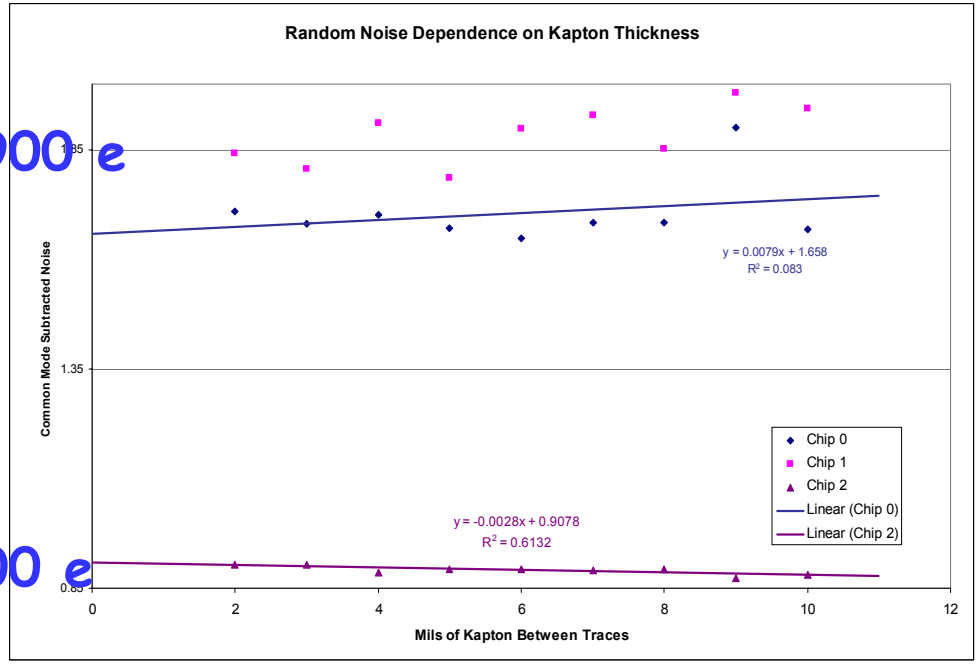


- See details in
  - http://d0server1.fnal.gov/users/kazu/www/smt2b/meetingUW.pdf

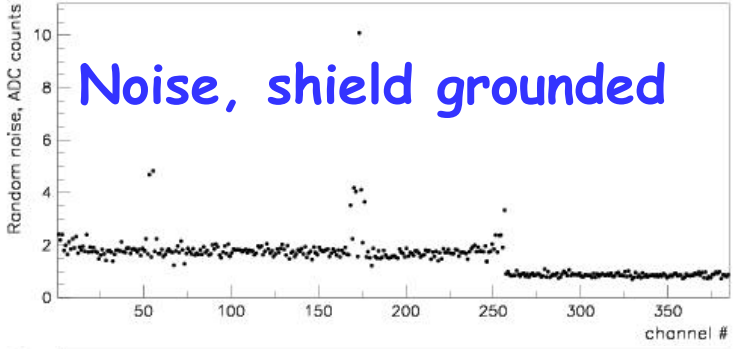
Analog Flex Cables

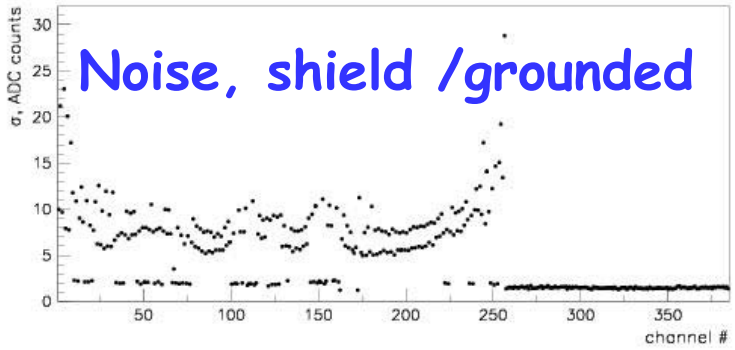
- Noise studies
  - Noise vs. two cables separation
  - Shielding effects
  - Noise vs. distance to shielding





Noise vs two cable separation



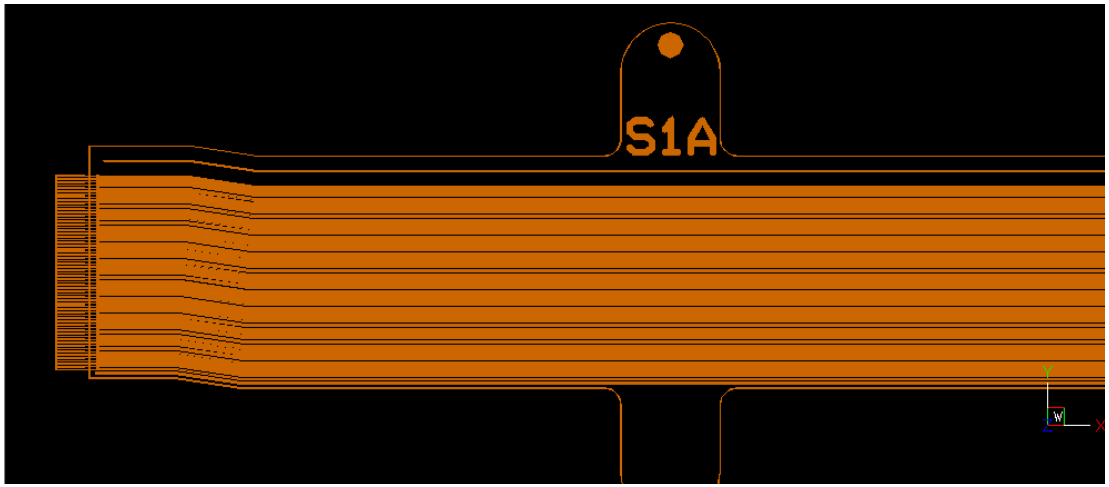


Rev.2 Analog cable

- Designed cable suitable for L0 support structure
  - Two types of lengths
  - Has a jog

L0 Analog Cables

- Received 40 new cables in March 03, all good
- Trace width 19 um, capacitance 0.35 pF/cm (Frank L, Kazu H)
- Dyconnex trying lamination of 2 cables with kapton mesh as spacer and ceramic piece to support bonding

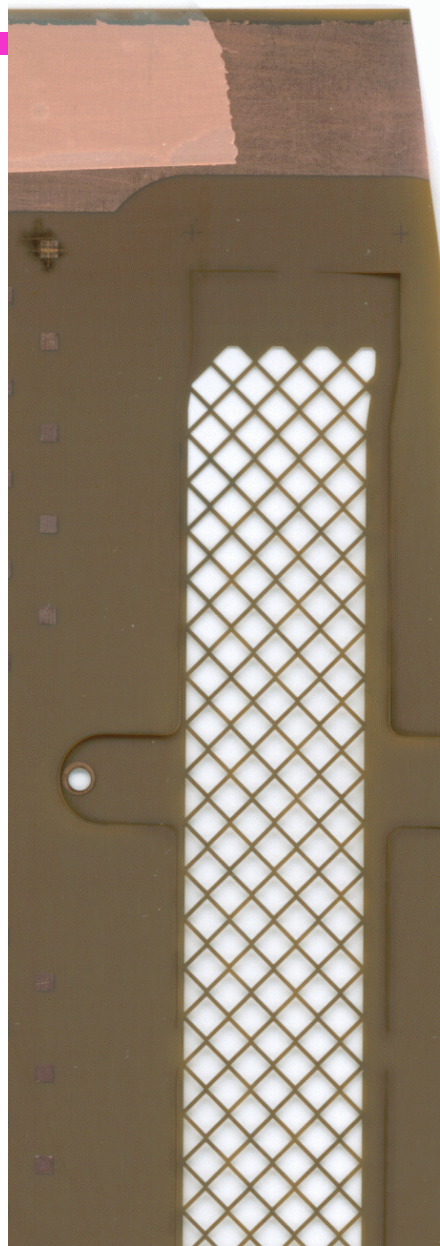


- See details in
  - http://d0server1.fnal.gov/projects/run2b/Silicon/Readout/L0/dyconex_status_march2k3.pdf

L0 module spacer

- Spacer needed to separate two analog cables by more than their thickness

- Received from Compunetics new kapton spacers
- Started assembly of two more modules with these spacers



L0 modules

- 5 L0 modules with earlier version of components

- Built 4 L0 modules with rev.2 hybrids
- 2 installed at the UW support structure